MST® Smart Profile (SP) Devices for Ron-BV improvement

Hideki Takeuchi

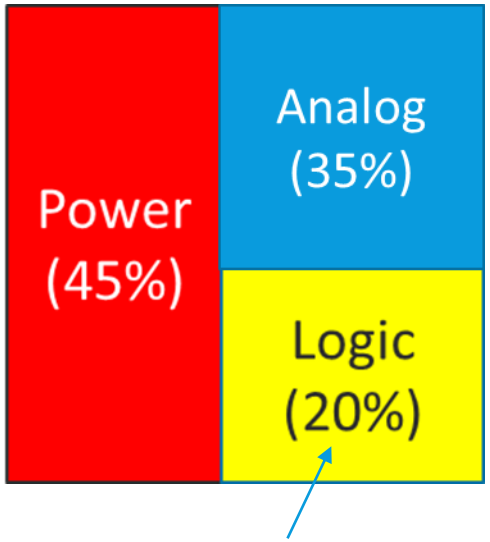
Outline

- Motivation — MST SP (smart profile) device concept
- MST SP 5V Device experimental data
- Roadmap

PMIC improvement strategy

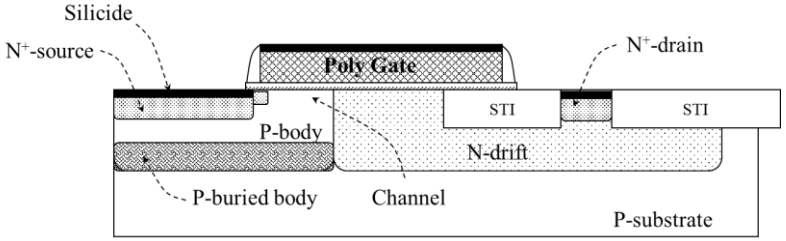
- Core Logic devices
  - Min. design rule: not possible to shrink
- Power switches
  - Large MOS transistors, not limited by lithography, possible to shrink
  - Wide voltage range in applications
- R_{DS}(on) improvement via MST
  - R_{ch} reduction via mobility improvement
  - R_{ch} is dominant at lower voltages
  - 5V devices are important for mobile applications

Typical 5V PMIC breakout



Minimum design rule
Established PDK

LDMOS R_{DS}(on) breakout



$$R_{DS}(on) = R_{DS,ext} + R_{Ch} + R_{N-drift}$$

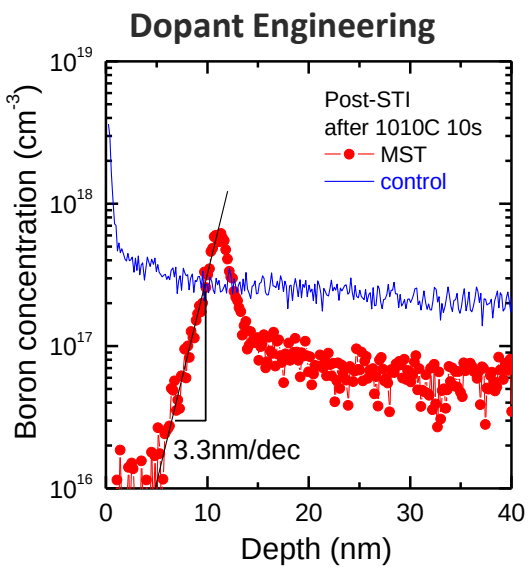
Extrinsic Source/Drain Resistance Effects — Intrinsic MOSFET Channel Resistance — N-drift Region Resistance Effects

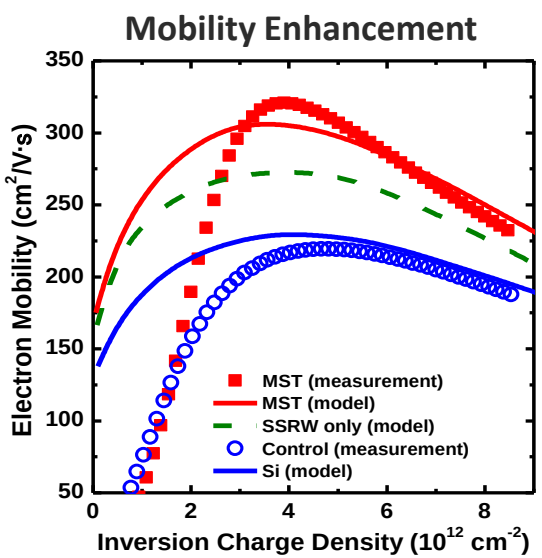
$$R_{DS}(on) = \frac{\rho_{SD,ext}}{W_{eff}} + \frac{L_{eff} t_{ox}}{W_{eff}\left(V_{GS} - V_T\right)\mu_{eff}\varepsilon_0\varepsilon_{ox}} + R_{S,N-drift}\left(\frac{L_{N-drift}}{W_{eff}}\right)$$

Estimate from LHC

MST® for R_{DS}(on) improvement

atomera





$$R_{DS}(on) = R_{DS,ext} + R_{Ch} + R_{N-drift}$$

Extrinsic Source/Drain Resistance Effects

Intrinsic MOSFET Channel Resistance

N-drift Region Resistance Effects

$$R_{DS}(on) = \frac{\rho_{SD,ext}}{W_{eff}} + \frac{L_{eff} t_{ox}}{W_{eff}\left(V_{GS} - V_T\right)\mu_{eff}\varepsilon_0\varepsilon_{ox}} + R_{S,N-drift}\left(\frac{L_{N-drift}}{W_{eff}}\right)$$

- MST improves long-channel mobility
- Can we boost mobility for short-channel performance via Dopant Engineering?

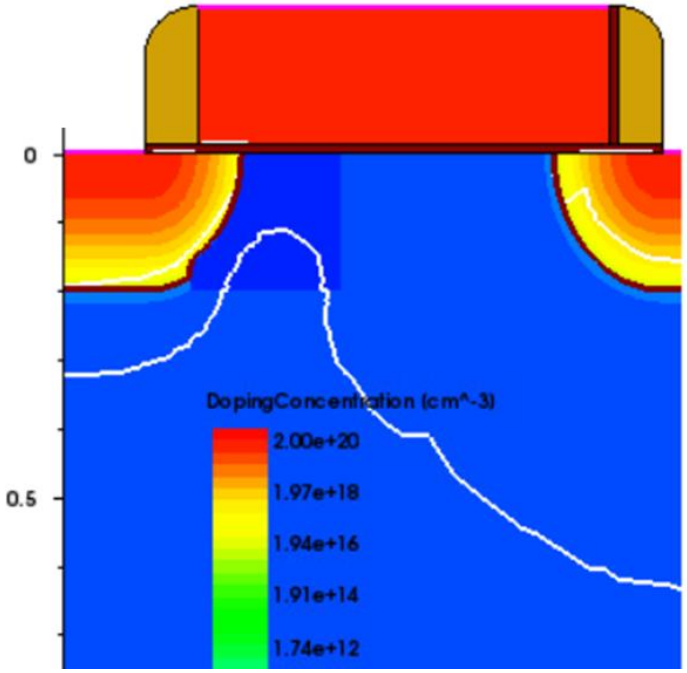
[1]: N. Xu et al., "Electron mobility enhancement in (100) oxygen-inserted silicon channel ," APL 107, 123502 (2015)
[2]: R.J Mears et al; "Simultaneous carrier transport enhancement and variability reduction in Si MOSFET by insertion of partial monolayers of Oxygen", IEEE VLSI Tech Symp. 2012

MST Smart Profile (SP) device concept

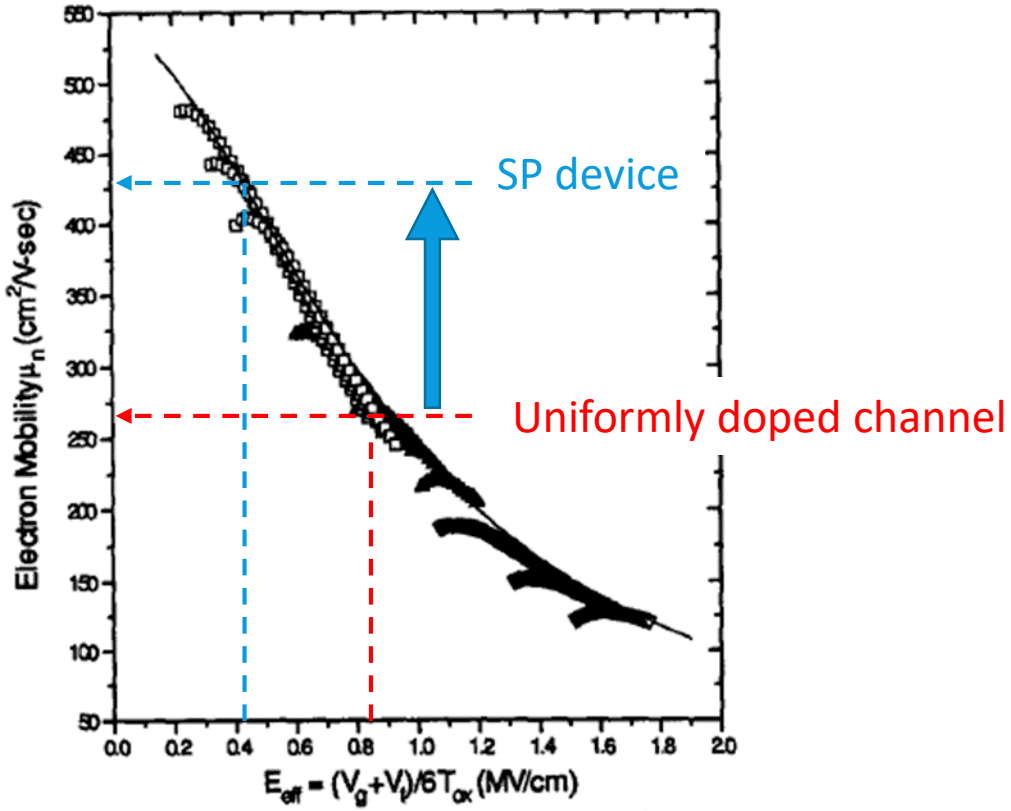
atomera

5V Device doping design for enhancing mobility

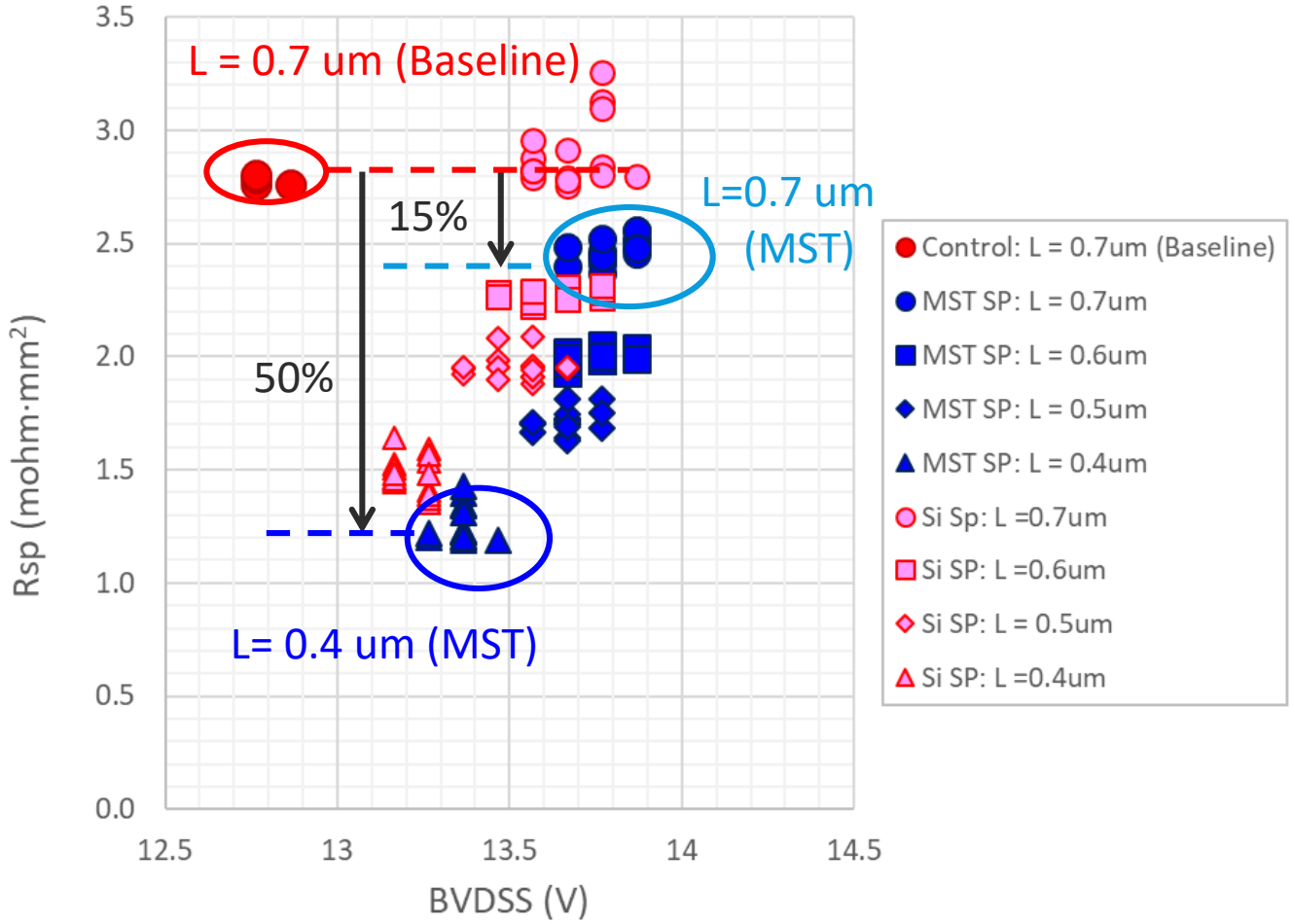
- Get rid of channel dopant
- Control Vt by source-side halo



Mobility vs. effective field

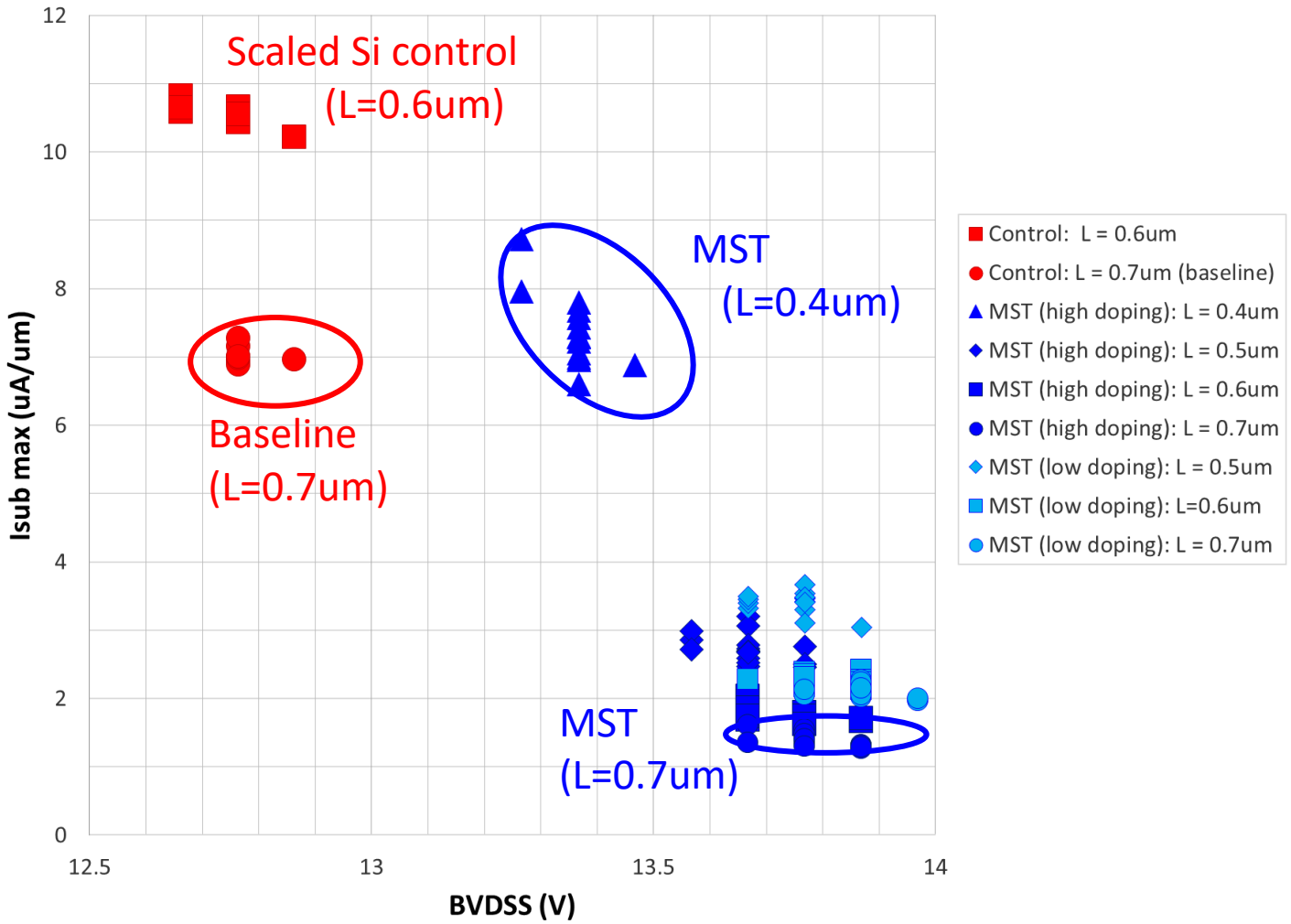


MST SP 5V Device Silicon Data: R_{sp} vs BVDSS



- **Lg=0.7um (baseline)**
  - Si SP device yields no R_{sp} reduction
  - MST SP device yields 15% R_{sp} reduction
- **Lg= 0.4um**
  - MST SP yields 50% R_{sp} reduction over Baseline device and 10% over Si SP
- **R_{sp} calculation method**
  - R_{sp} = Vds/Idlin * Ldevice
  - Ldevice = Lg + 0.52um
  - 0.52um = 2* (contact to poly pitch in 180nm node)

MST SP 5V Device Silicon Data: I_{submax} vs BVDSS



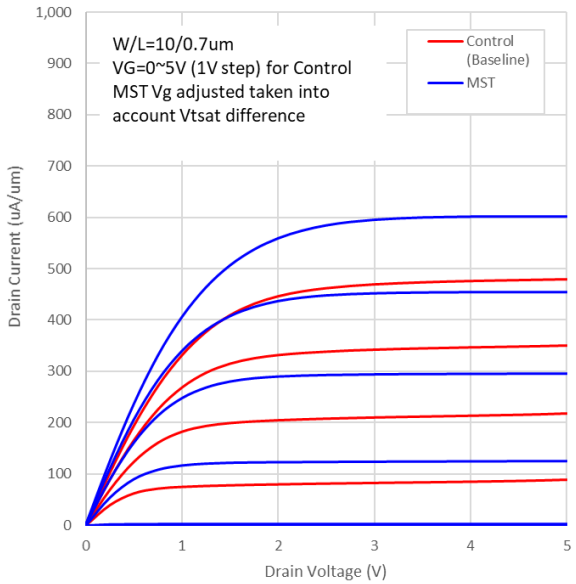
- Reduced channel doping improves I_{sub} max and BV characteristics
- BVDSS and I_{sub} max of MST SP L=0.4um device is comparable to that of Baseline L=0.7um

MST SP 5V device Silicon Data: Output Characteristics

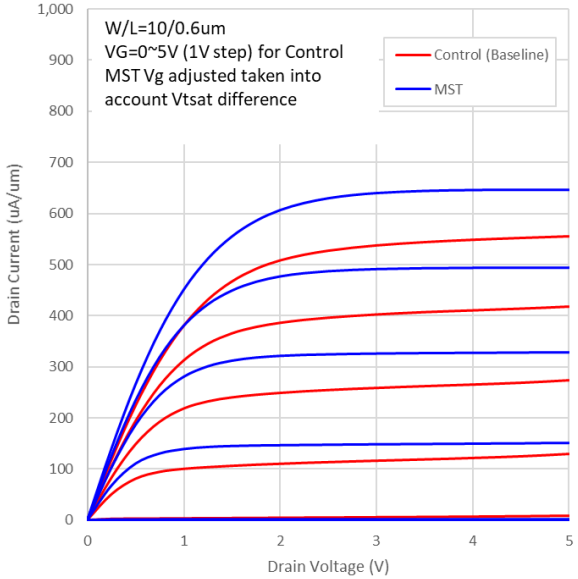
atomera

MST SP device yields good performance improvement at target Lg and also provides better Lg scalability

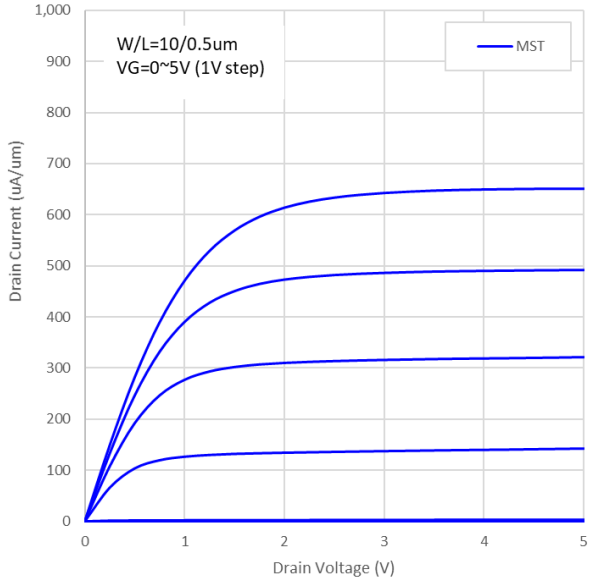
L=0.7um



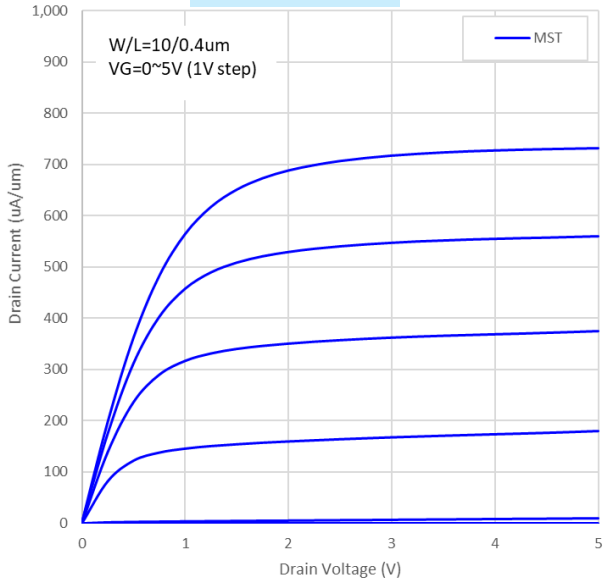
L=0.6um



L=0.5um



L=0.4um



Gm	+30%
Idlin	+20%
Idsat	+25%

Rout	+122%
Gm·Rout	+189%

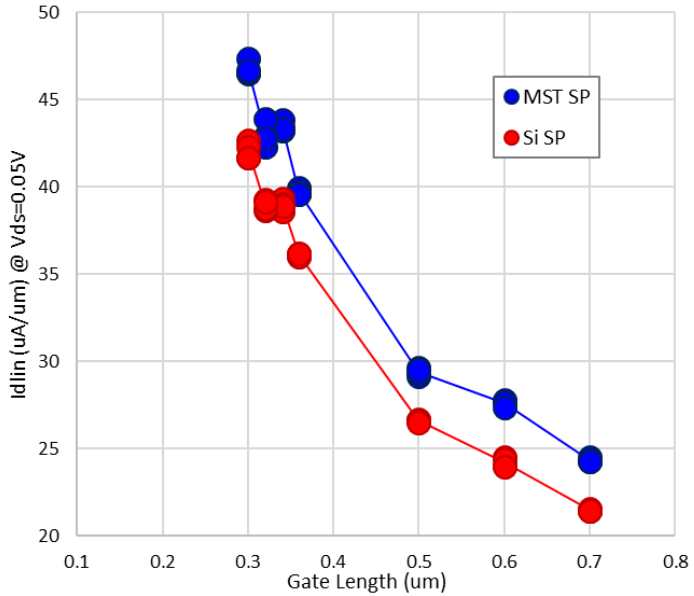
Control (baseline) devices not functional at L=0.5um & 0.6um

MST SP 5V Device : Progress after 1st Silicon

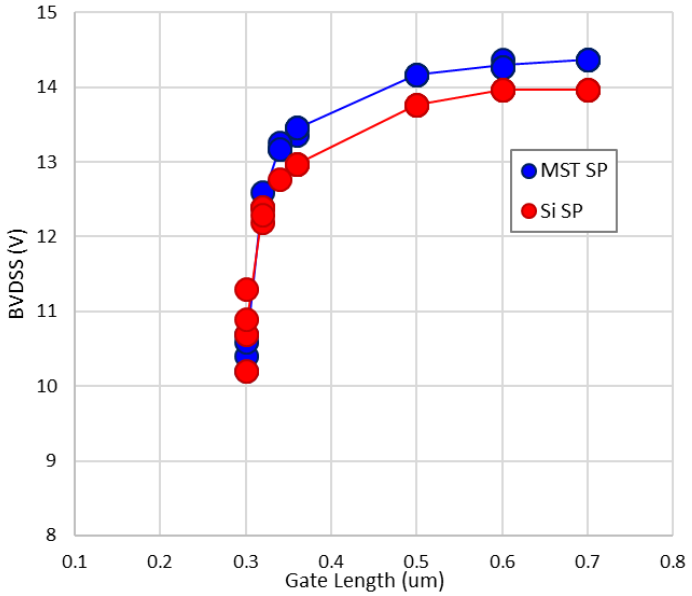
atomera

MST SP 5V device shows 10% improvement in both Idlin and Isub_max

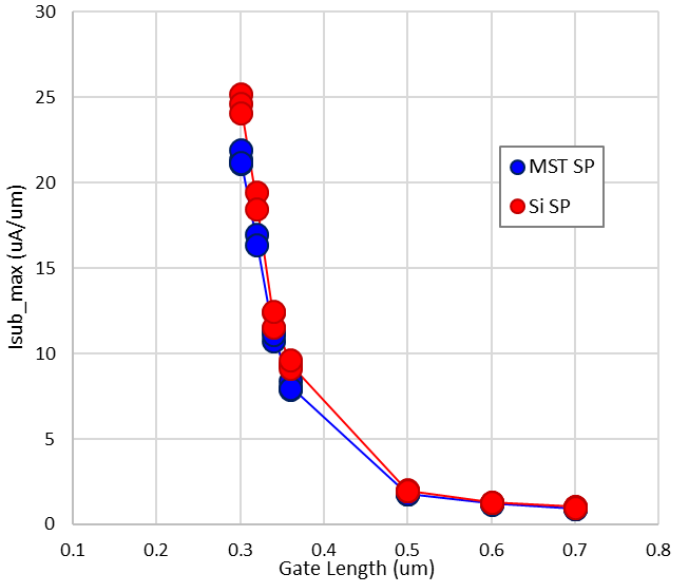
Idlin vs. Lg



BVDSS vs. Lg



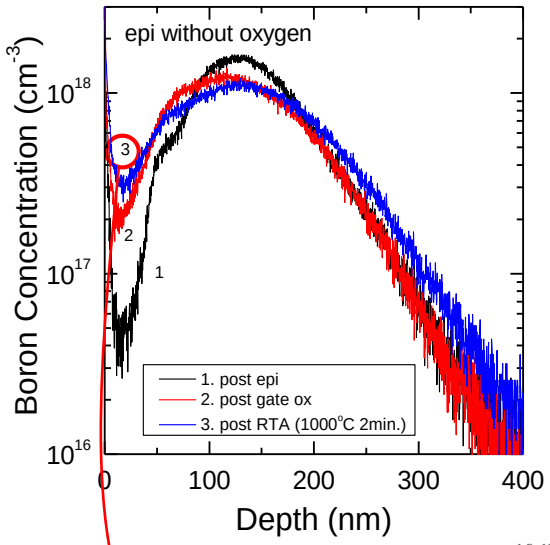
Isub max vs. Lg



Simultaneous Dopant Peak Anchoring and SSR channel formation by MST (trapping interstitials)

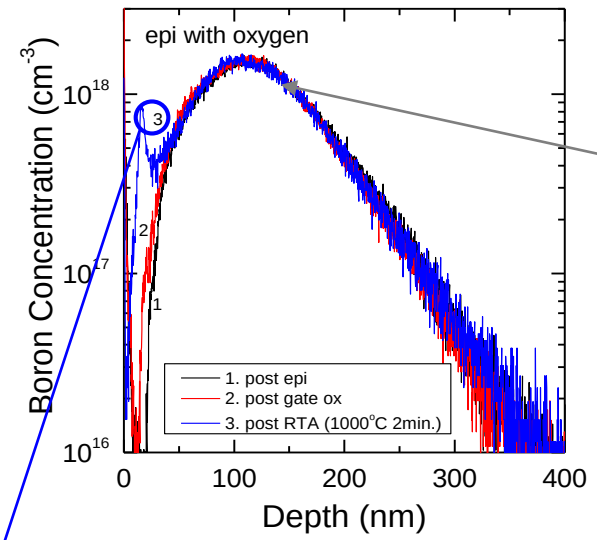
atomera

Boron SIMS of Si epi without OI layer

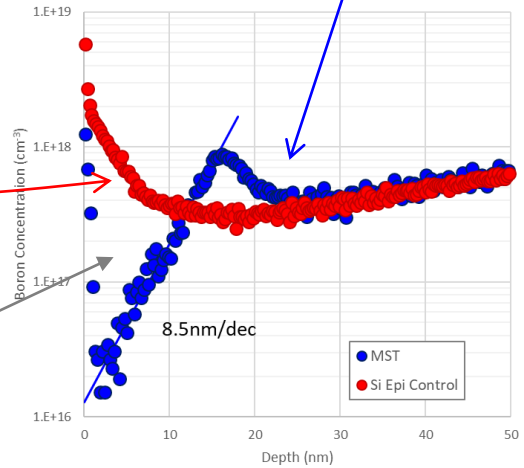


MST blocks interstitial diffusion

Boron SIMS of MST



MST film can retain Well implant peak



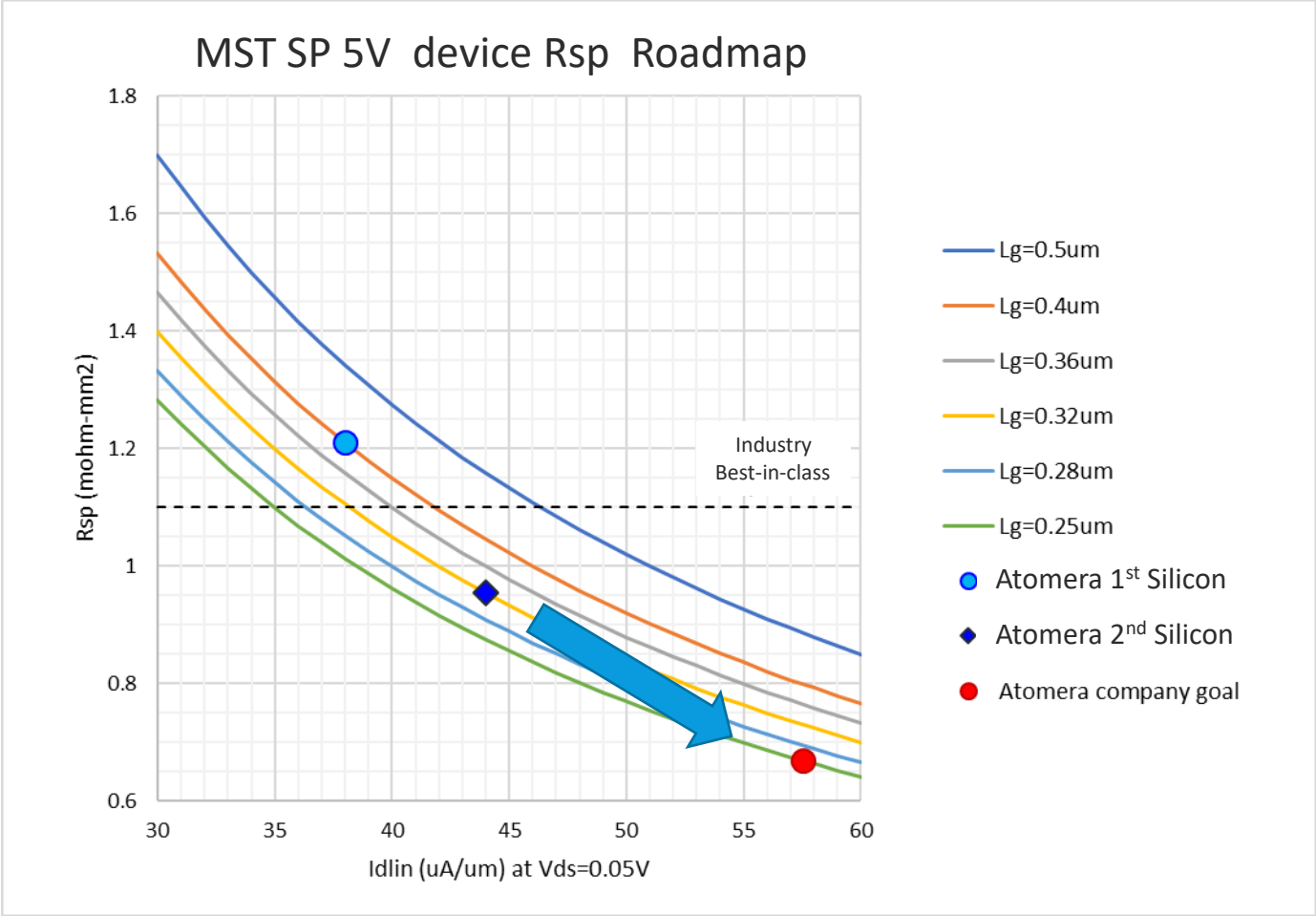
MST can retain surface undoped channel through process

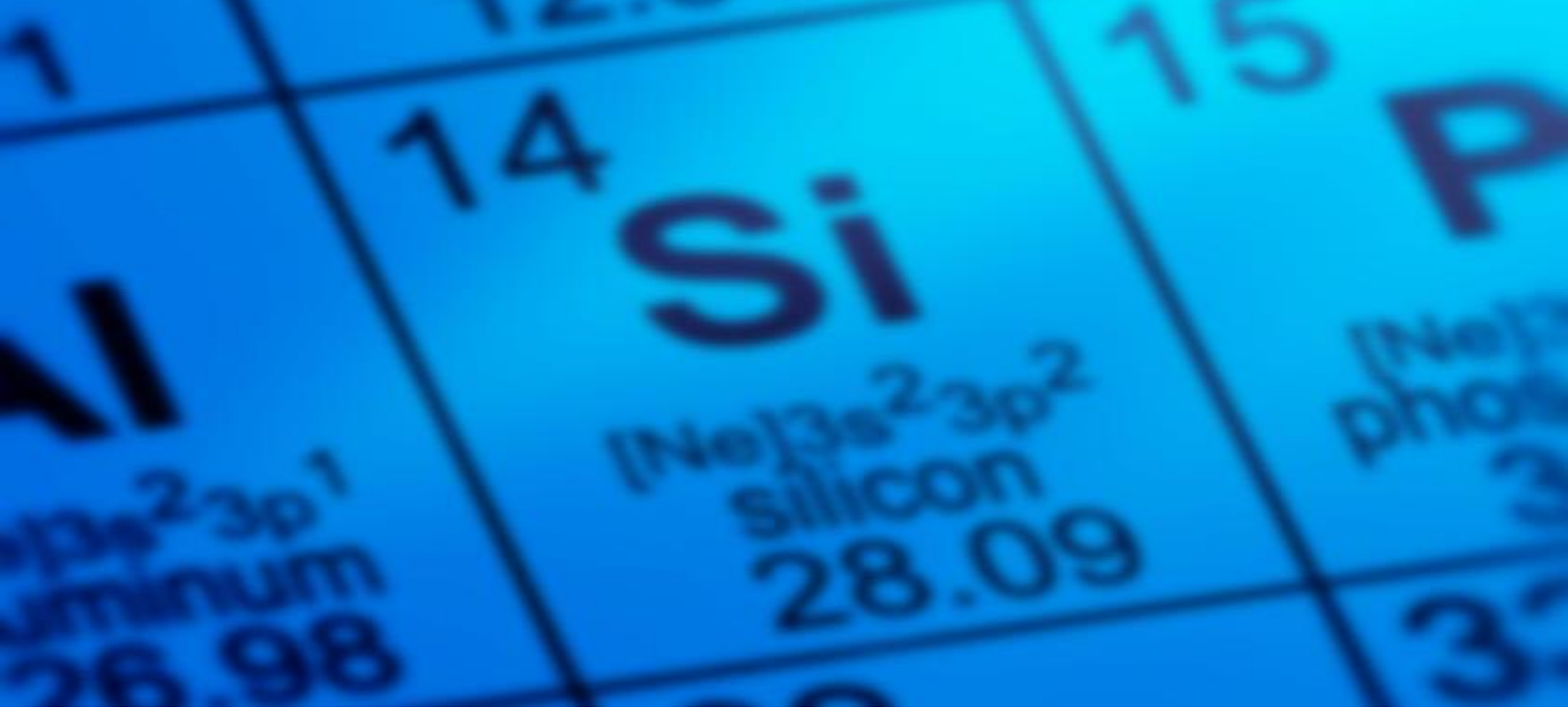
Implant-defined dopant peak smears out due to OED (oxidation-enhanced diffusion) for regular Si

- Gate oxidation injects Si interstitials
- Boron and phosphorus diffusion is mediated by Si interstitials

Ref: See Paper 4B-2 EDTM 2017

MST SP 5V device performance roadmap





atomera