MST® Process Modeling with Sentaurus TCAD

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MST Structure
**MST Layer Planar Schematic**

- **MST Oxygen Insertion (OI) plane** shown
- Planar insertion of oxygen into Si lattice.
- **metastable**: O emitted during thermal cycles.

*cartoon sketch: OI plane*
MST Vertical Layer Structure

- multiple oxygen inserted layers
- Si between OI layers
- different than SiO₂.
SIMS Modeling

- comparing simulation to experiment: experiment uses SIMS, so simulation should also be “SIMSified”
- Sentaurus: no model for SIMS
- Gautier: described linear model for SIMS artifact
- post-processing: convolutions implemented with S-Visual

Deconvolution of SIMS Depth Profiles of Boron in Silicon

- Gautier (1996): represent SIMS effect as convolutions
- Convolution 1: normal Gaussian with standard deviation $\sigma$, peak $(2\pi\sigma^2)^{-1/2}$
- Convolution 2: unit two-sided exponential with $\lambda_1$, $\lambda_2$, peak $(\lambda_1 + \lambda_2)^{-1}$
Oxygen SIMS modeling

- **SIMS**: combination of free and interface oxygen
- **model**: trapped oxygen @ interface, plus free oxygen
- **Gautier convolution kernel** matches experimental peak.
- **free oxygen** to match remaining profile
Process Mechanisms

Process Mechanisms
Interstitial Trapping

- **perpendicular** to OI plane.
- **lattice distortion** out-of-plane
- **Local tensile strain**: gaps for Si interstitials.
- **Local compressive strain**: stress relieve by Si vacancies.
- **Result**: point “trapped” by OI layers, then “recombine”.

**cartoon sketch: vertical**
Trapping: Density Functional Theory
Process Mechanisms

(a) trapped oxygen  
(b) trapped interstitial  
(c) trapped vacancy  
(d) trapped dopant  
(e) oxygen emission  

(f) oxygen capture  
(g) interstitial capture  
(h) interstitial emission  
(i) vacancy capture  
(j) vacancy emission  

(k) V-I recombination  
(l) dopant trapping  
(m) dopant emission  
(n) oxygen diffusion  
(o) dopant diffusion
linear kinetic equations

- **Interstitial trapping (f), from each side:**
  Trapping rate = \( k_{\text{trapI}} O_{\text{trapI}} I_{\text{free}} \)

- **Vacancy trapping (g), from each side:**
  Trapping rate = \( k_{\text{trapV}} O_{\text{trapV}} V_{\text{free}} \)

- **Oxygen trapping (e), from each side:**
  Trapping rate = \( k_{\text{trapO}} O_{\text{trapO}} O_{\text{free}} \)

- **Oxygen emission (d), to each side:**
  Emission rate = \( k_{\text{emitO}} O_{\text{trapO}} / 2 \)

- **activation energy:** oxygen same, point defects zero

- **oxygen diffusion** retarded proportional to OI oxygen
  \( \Delta O_{\text{free}} = k_{\text{diffO}} O_{\text{trapD}} \nabla O_{\text{free}} \)
Model Calibration

Model Calibration
MST Boron Marker Experiments

Oxygen ambient

- Silicon cap
- Boron marker
- Silicon buffer
- OI layers
- Silicon buffer
- Boron marker
- Silicon substrate

Graph showing boron concentration [10^{19}/cm^3] vs depth [nm].
Control no MST/ OI: Boron Oxygen-Enhanced-Diffusion

- both peaks diffuse: interstitials reach both markers.
- 850C anneal: peaks merge.
With MST OI layers: OED suppression

- **Surface peak**: oxidation-enhanced diffusion (OED).
- **Buried peak**: very little diffusion.
- **Central peak**: boron was unintentionally trapped in OI during deposition.
MST OI layer modeling
Modeling Boron Implantation Experiment

- epitaxy followed by implant then anneal
- interstitial trapping reduced relative to marker experiment
- demonstrates boron trapping in addition to interstitial trapping
- insensitive to vacancy trapping
Modeling Phosphorus Implantation Experiment

- epitaxy followed by implant then anneal
- interstitial trapping reduced relative to marker experiment
- demonstrates boron trapping in addition to interstitial trapping
- insensitive to vacancy trapping
50 nm PDSOI w/ MST OI layers: trapped boron and phosphorus
PDSOI: Long-channel cut
35 nm CMOS application

control case  
w/ MST OI layers

• gate oxidation, polysilicon oxidation changed from deposited to grown
• interstitial injection during polysilicon oxidation 10× (RSCE calibration)
35 nm CMOS: improved PFET short-channel

- trapped dopant modeled as surface charge
- S-Device simulation: $\delta$-potential excluded
- reduced DIBL with MST OI layers
- boron diffusion retarded by interstitial trapping
5V NFET Breakdown: current contours

- MST layers move doping from the interface
- trapped dopant in the MST layer is not rendered here.
5V NFET Breakdown: current contours

- linear current scale
- At the breakdown condition (100 nA/µm), current peak in MST structure is focused at MST layers.
- in control device, current peak is closer to surface.
- result: 1.2 V increase in $V_{BDSS}$
Summary

- MST OI layers are sheets of oxygen inserted into Si lattice
- process modeling with S-Process
- trap dopants, directly immobilizing them
- trap point defects, reducing dopant diffusion
- result: steeper surface doping profiles; anchoring of implant dopants
- application example: doping control for improved CMOS scaling