

# Oxygen-Inserted SegFET: A Candidate for 10-nm Node System-on-Chip Applications

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## Abstract

An oxygen-inserted quasi-planar segmented channel MOSFET design is proposed and studied for monolithic system-on-chip applications. Projections indicate that it will provide for higher performance than bulk FinFET technology at the 10 nm node, due to higher field-effect carrier mobility, lower source/drain series resistance, and the benefit of super-steep retrograde well punchthrough-stopper doping.

## Introduction

Planar bulk MOSFET performance variability and OFF-state leakage ( $I_{OFF}$ ) worsen as the gate length ( $L_g$ ) is scaled down below 30 nm, due to increased channel doping and worsening electrostatic integrity (EI), respectively. Thin-body transistor structures such as the FinFET have been adopted to address these issues, but with the trade-off of larger source/drain resistance ( $R_{s/d}$ ) resulting in lower cutoff frequency (cf. Fig. 1) [1]. Another drawback of FinFET technology is that it is not straightforward to achieve multiple (significantly different) values of threshold voltage ( $V_T$ ), due to the relatively weak dependence of  $V_T$  on fin dopant concentration [2]. These issues pose challenges for implementation of mixed-signal systems-on-chip (SoCs), which will be the main driver for technology development in the era of mobile electronics. To circumvent these issues, the segmented-channel MOSFET (SegFET) structure was recently proposed and demonstrated, comprising quasi-planar Si strips in the channel region to enhance EI while maintaining low  $R_{s/d}$  [3]. This structure can easily incorporate “oxygen-insertion” (OI) technology [4, 5] to boost carrier mobilities and further improve EI by facilitating the formation of a super-steep retrograde-well (SSRW) doping profile as shown in Fig. 2. This paper compares n-channel device performance for bulk OI-SegFET and FinFET structures at the 10 nm node, with a focus on multiple- $V_T$  capability and analog/RF performance metrics.

## Device Modeling and Simulation

Three-dimensional (3D) device simulations were performed using *Sentaurus* TCAD software as described in [5, 6]. Electron mobility enhancement was modeled analytically, taking into account sub-band re-occupation among multiple valleys under quantum confinement. OI regions are modeled as wide-bandgap material with 0.6 eV band-edge offsets to the conduction and valence bands of Si, based on the calibrated numerical simulations in previous work [4]. Fig. 3 shows the analytically modeled electron field-effect mobility w/ and w/o OI, agreeing well with the experimental and numerical results in [4]. Due to the larger bandgap of the OI layers, band-to-band tunneling (BTBT) junction leakage current is reduced, as shown in Fig. 4. The OI-SegFET has segmented channel and lightly doped shallow source/drain extension regions to improve EI, and heavily doped raised source/drain regions to achieve low  $R_{s/d}$  similarly to a planar bulk MOSFET, as shown in Fig. 5. It should be noted that the Si strip height ( $H_{strip}$ ) is not a critical design parameter; it can be equal to or less than the thickness of the lightly doped channel region ( $T_{Si}$ ), allowing for variability in the fabrication process [7].

Design parameter values relevant for the 10 nm technology node (listed in Tab. I) were used for the device simulations.

## Results and Discussion

Multiple  $V_T$  values can be facilitated by using shorter  $L_g$  for high-performance (HP) devices and longer  $L_g$  for low-power (LP) devices. Fig. 6 shows simulated transfer characteristics for bulk FinFETs with shorter  $L_g$  and lighter background channel/fin doping for HP application, and longer  $L_g$  with heavier background channel/fin doping for LP application, for 2 peak values of punchthrough-stopper doping ( $N_{peak}$ ) with 10 nm/dec gradient [7]. Different gate work function values were used for the 2  $N_{peak}$  cases in order to match LP  $I_{OFF}$  values. These results show that  $N_{peak}$  cannot be too high if multiple values of  $V_T$  are to be achieved via fin doping and  $L_g$  tuning, and that relatively high fin doping is needed to achieve high  $V_T$ . In contrast, for the OI-SegFET, low channel doping values can be used for both LP and HP devices, with back biasing as an additional knob for adjusting  $V_T$ , as summarized in Tab. II.

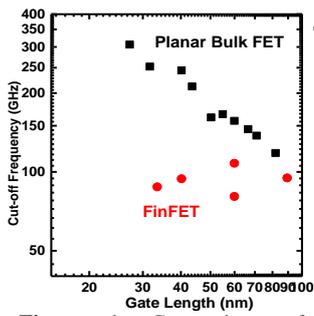
Fig. 7 compares the simulated FinFET and OI-SegFET currents normalized to layout width. (Note that the FinFET has larger effective channel width than the OI-SegFET.) For HP applications, the two structures offer comparable performance; for LP devices, performance is worse for the FinFET, likely due to strong *Coulombic* scattering and lower electron effective mobility, which is consistent with the degraded FinFET transconductance ( $G_m$ ) seen in Fig. 8. Thanks to the SSRW profile, the OI-SegFET is projected to offer better energy vs. delay performance than the FinFET, as shown in Fig. 9. Pertinent to analog/RF performance, Fig. 10 shows that OI-SegFETs have larger transconductance efficiency ( $G_m/I_d$ ) than FinFETs, due to better sub-threshold performance and smaller ON-state resistance. Fig. 11 shows that OI-SegFETs can achieve higher cut-off frequency ( $f_T$ ) than FinFETs, due to higher  $G_m$  and smaller  $R_{s/d}$ .

## Conclusion

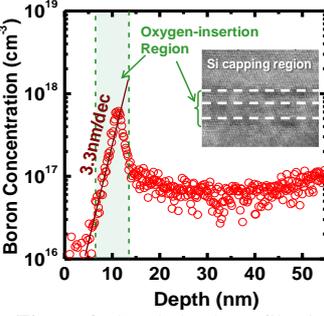
At the 10 nm technology node, the SegFET transistor design combined with oxygen-insertion technology can achieve significantly higher performance than the bulk FinFET design, for multiple values of  $V_T$  and analog/RF applications. Hence it is a promising candidate for future low-cost monolithic SoCs.

## References

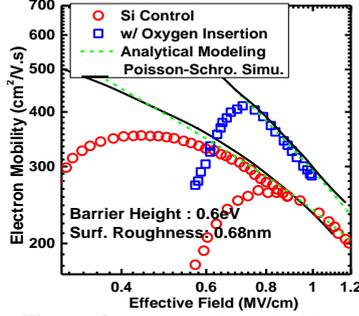
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- [3] B. Ho *et al.*, “First Demonstration of Quasi-Planar Segmented-Channel MOSFET Design for Improved Scalability,” *IEEE Transactions on Electron Devices*, vol.59, no.8, pp.2273-2276, 2012.
- [4] N. Xu *et al.*, “MOSFET Performance and Scalability Enhancement by Insertion of Oxygen Layers,” *IEEE International Electron Device Meeting Tech. Dig.*, pp.127-130, 2012.
- [5] N. Xu *et al.*, “Extension of Planar Bulk N-Channel MOSFET Scaling with Oxygen Insertion Technology,” to appear in *IEEE Transactions on Electron Devices*, 2014.
- [6] *Sentaurus Device User Guide*, version 2013.12.
- [7] X. Sun *et al.*, “Tri-Gate Bulk MOSFET Design for CMOS Scaling to



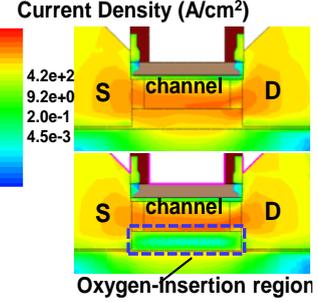
**Figure 1:** Comparison of planar bulk MOSFET and FinFET cut-off frequency ( $f_r$ ) vs. gate length ( $L_g$ ), after [1].



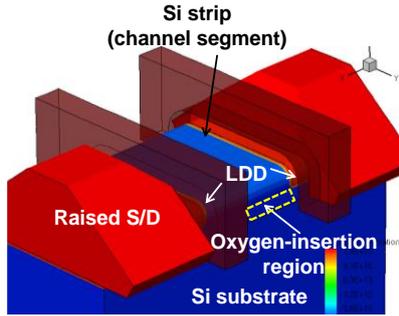
**Figure 2:** SIMS depth profiles in the N-channel region with OI by selective epitaxy after all CMOS thermal process steps.



**Figure 3:** Measured (symbols) and simulated (lines) field-effect electron mobility vs. effective transverse electric field for long-channel N-MOSFET w/OI vs. Si control.



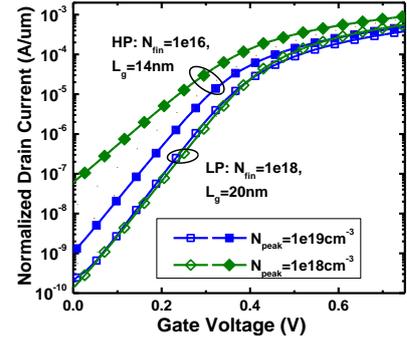
**Figure 4:** Simulated OFF-state current density in MOSFETs w/o (top) and with energy barriers (bottom), showing the benefit of OI for reducing BTBT current.



**Figure 5:** Schematic illustration of the quasi-planar segmented-channel MOSFET (SegFET) structure incorporating an oxygen-inserted (OI) region at the base of the gated channel region. (The gate electrode is not shown, for clarity.)

$L_g$	14nm (HP)	20nm (LP)
$EOT$	0.95nm	
$V_{DD}$	0.72V	
Gate Pitch	70nm	
Strip Pitch	36nm	
	<b>FinFET</b>	<b>OI SegFET</b>
$W_{Fin}$	9nm	$W_{strip}$
$H_{Fin}$	22.5nm	$H_{strip}$
		28nm
		7nm

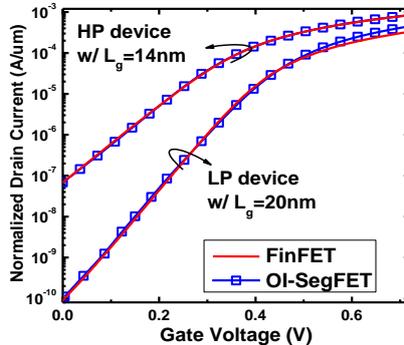
**Table I:** Key device design parameter values for 10 nm-node bulk FinFET and OI-SegFET structures studied in this work.



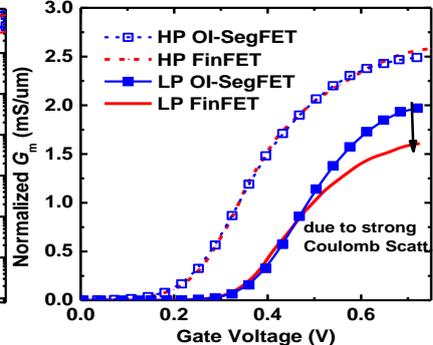
**Figure 6:** Simulated normalized  $I_d$  vs.  $V_g$  curves for 10 nm-node bulk FinFETs, showing that the punchthrough-stopper peak doping should be low to allow for  $V_T$  adjustment via fin doping and  $L_g$  tuning.

$L_g$	14nm (HP)	20nm (LP)
	<b>FinFET</b>	<b>OI SegFET</b>
HP channel doping	$1.0e16 \text{ cm}^{-3}$	$5.0e16 \text{ cm}^{-3}$
LP channel doping	$1.0e18 \text{ cm}^{-3}$	
SSRW peak doping	$1.0e18 \text{ cm}^{-3}$	$4.0e18 \text{ cm}^{-3}$
SSRW doping gradient	10 nm/dec	3.3 nm/dec
Metal Gate Workfunction	4.50eV	4.43eV
Body Biasing	--	$+V_{DD}/2$ (HP) $-V_{DD}/2$ (LP)

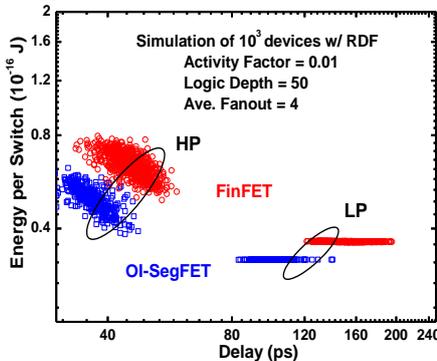
**Table II:** Optimized device design parameter values and back bias voltages for bulk FinFET vs. OI-SegFET, for high performance (HP) and low-power (LP) applications.



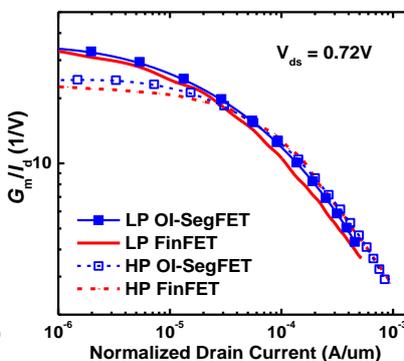
**Figure 7:** Comparison of normalized  $I_d$  vs.  $V_g$  curves for 10 nm-node FinFETs and OI-SegFETs, for the HP and LP designs listed in Table II.



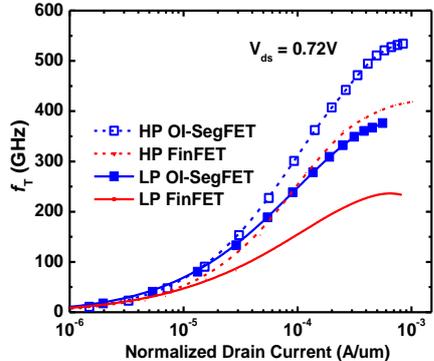
**Figure 8:** Simulated transconductance ( $G_m$ ) vs. normalized drain current characteristics for 10 nm-node bulk FinFET vs. OI-SegFET.



**Figure 9:** Simulated energy vs. delay for a 50-stage inverter chain implemented with 10 nm-node bulk FinFETs vs. OI-SegFETs, showing the impact of random dopant fluctuations.



**Figure 10:** Simulated transconductance efficiency ( $G_m/I_d$ ) vs. normalized drain current for 10 nm-node bulk FinFET vs. OI-SegFET.



**Figure 11:** Simulated  $f_T$  vs. normalized drain current for 10 nm-node bulk FinFET vs. OI-SegFET.