Effectiveness of Quasi-Confinement Technology for Improving P-Channel Si and Ge MOSFET Performance

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Abstract
The effectiveness of Quasi-Confinement technology for enhancing Si and Ge hole mobility in planar bulk MOSFET and FinFET structures is studied, for insight into the use of this technology for boosting nanoscale device performance.

Introduction
Quasi-Confinement (QC) technology recently was proposed for enhancement of carrier mobilities to sustain the historical pace of MOSFET performance enhancement when the benefits of strain saturate with device pitch scaling [1]. For Si, a QC potential can be realized by inserting oxygen sub-monolayers into the channel region, and the hole mobility is enhanced due to the separation of sub-band wavefunctions which results in reduced carrier scattering rates [1]. Interest in Ge for high-performance P-channel MOSFETs has grown due to its high bulk hole mobility [2-4]. Therefore, the effectiveness of QC technology for boosting the hole mobility in Ge MOSFETs is studied in this work. Comparisons against Si are provided for planar bulk MOSFETs as well as FinFETs relevant for future technology nodes.

Experimental
Planar MOSFETs with plasma-nitrided gate oxide were fabricated on (100) Si wafers using a conventional process flow, except that after shallow trench isolation, oxygen-inserted Si layers were grown selectively as described in [1] to form the QC region (Fig. 1). The O atoms are interstitially placed to minimize disruption to the Si lattice.

The Poisson-Schrödinger self-consistent simulation formalism was used to model the effect of inserted QC layers to perturb the carrier sub-band structures within the semiconductor channel region of a P-type MOSFET. The 6×6 $k \cdot p$ approach is adopted to calculate the inversion-layer hole sub-band structures [5]. The Kubo-Greenwood formula is used to calculate the field-effect mobility, considering phonon and surface roughness scattering mechanisms. Fig. 2 shows that the simulated (100) Si hole universal mobility curves match the experimental data across a wide temperature range [6]. The simulation is also calibrated to published experimental data for Ge hole mobility, as shown in Fig. 3 [2-4]. The QC layers are modeled as wide-band-gap layers (Fig. 4), with the energy barrier height and width used as fitting parameters.

QC Impact on Planar Bulk MOSFET Hole Mobility
Hole mobilities are extracted using the split-CV method, for a Si MOSFET with 2 sub-monolayer oxygen layers inserted in the channel region as well as a control device with no inserted layers, as shown in Fig. 5. The simulation results indicate that the modeling approach can be used to predict enhancements in Si hole mobility, with a QC barrier height (ΔE) value of 0.6 eV. Fig. 6 shows the wavefunction magnitudes for the 3 lowest sub-band pairs from the Si valence band. It is clearly seen that the QC layers effectively separate the high-energy sub-band wavefunction from the low-energy sub-band wavefunction; this results in reduced *inter-sub-band* scattering rates.

For Ge channel material, Fig. 7 shows the simulated hole mobility for various values of QC barrier height and capping layer thickness. If the QC barrier height is the same as that induced by insertion of oxygen sub-monolayers in Si (*i.e.* ΔE = 0.6 eV), then hole mobility is degraded for QC-Ge as compared to Ge; however, if ΔE is reduced to 0.2 eV and the Ge capping layer thickness is increased to 5 nm, hole mobility is enhanced for QC-Ge. The sub-band wavefunction magnitudes for Ge shown in Fig. 8 suggest that smaller ΔE also can be effective for reducing *inter-sub-band* scattering rates. On the other hand, smaller ΔE results in a wider wavefunction distribution (*i.e.* more wavefunction penetration into the QC regions), resulting in lower *intra-sub-band* scattering rates, which turns out to have more impact on Ge hole mobility than on Si hole mobility.

QC Impact on P-Channel FinFET Performance
Because quantum confinement in ultra-thin channel regions is known to be beneficial for (110) holes [5] and QC can mitigate the degradation of FinFET electrostatic integrity due to volume inversion [1], QC technology is expected to boost the performance of aggressively scaled P-channel FinFETs. Fig. 9 illustrates how QC can be implemented with the FinFET structure, by starting with a 4-nm-wide QC fin and epitaxially growing the capping layer on the fin sidewalls. Listed in the table are the device design parameter values assumed for future CMOS technology nodes; the final fin width (W_{Fin}) is varied by changing the thickness of the capping layer. Figs. 10 and 11 show that the benefit of QC technology for enhancing Si FinFET hole mobility and transconductance (normalized to channel form factor W/L_g and drain bias V_{ds}), respectively, is sustained with scaling. However, Figs. 12 and 13 show that benefits for Ge FinFETs are only seen for the first projected node. This is likely due to the fact that Ge hole mobility is more limited by *intra-sub-band* scattering and therefore is more vulnerable to quantum confinement effects than Si hole mobility.

Conclusion
Calibrated simulations show that for a given channel surface crystalline orientation (corresponding to a planar MOSFET or a vertical FinFET), the QC barrier height and capping layer thickness can be co-optimized to provide for enhanced Ge hole mobility. QC technology provides a pathway for boosting the performance of P-channel FinFETs with aggressively scaled device pitch.

References
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[4] S. Takagi *et al.*, "Hole Mobility enhancement of p-MOSFETs using global and local Ge-channel technologies," *MSE-B*, 135, p.250, 2006.
[5] N. Xu *et al.*, "Carrier Mobility Enhancement via Strain Engineering in Future Thin-Body MOSFETs," *IEEE EDL*, 33, p.318, 2012.
[6] S. Takagi *et al.*, "On the Universality of Inversion Layer Mobility in Si MOSFET's," *IEEE T-ED*, 41, p.2357, 1994.
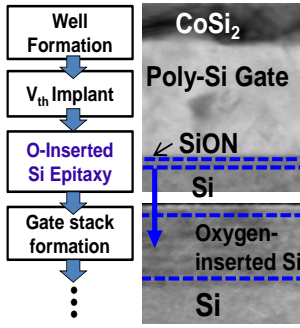
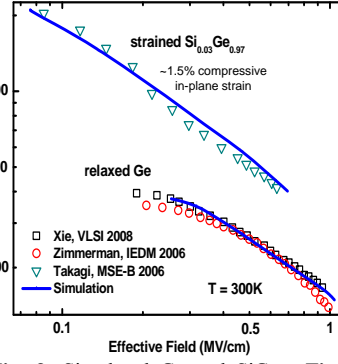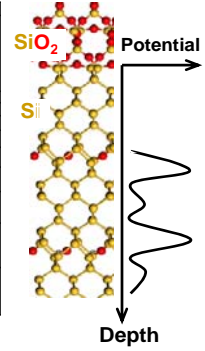**Fig. 1:** TEM cross-sectional view of a fabricated Si MOSFET with oxygen sub-monolayers inserted.
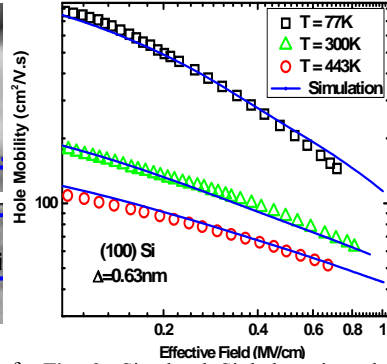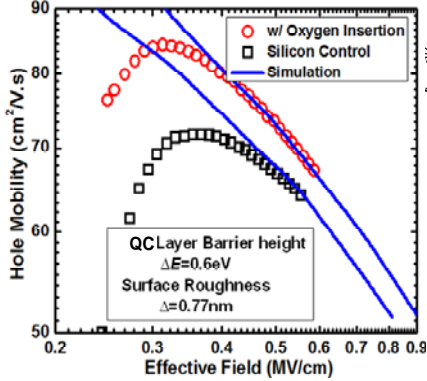

Fig. 2: Simulated Si hole universal mobility curves compared to experimental results from [6].
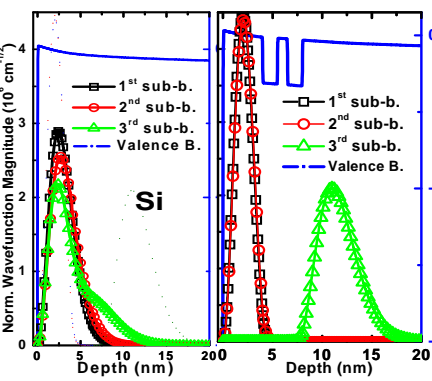

**Fig. 3:** Simulated Ge and SiGe hole mobility curves compared to experimental results from [2-4].

**Fig. 4:** Illustration of model for insertion of sub-monolayers to achieve quasi-confinement (QC).

Fig. 5: Simulated Si hole mobilities compared to experimental results, for bulk-Si MOSFET w/ and w/o QC layers inserted.


Fig. 6: Simulated hole sub-band wavefunction magnitudes for bulk-Si MOSFET w/o (left) and w/ (right) QC layers inserted.
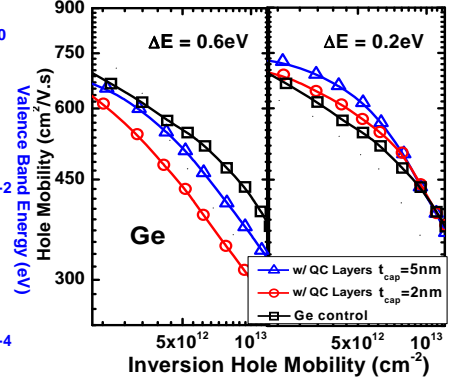

Fig. 7: Simulated Ge hole mobilities *vs.* inversion hole concentration, for devices w/ and w/o QC layers inserted.
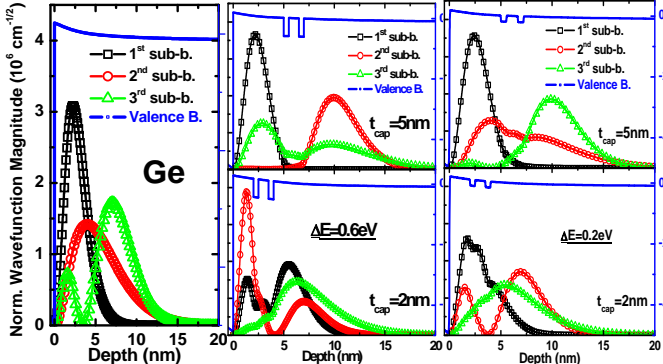

Fig. 8: Simulated hole sub-band wavefunction magnitudes for bulk-Ge MOSFETs: control (left) and w/ QC using various values of barrier energy and capping layer thickness (middle, right).
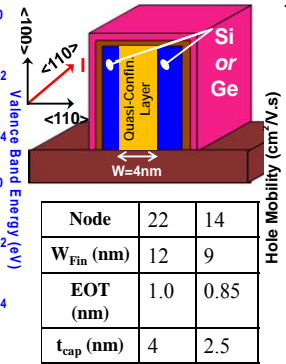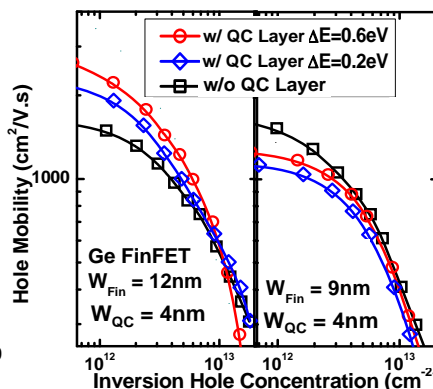

Fig. 9: Illustration of FinFET structure with QC layer incorporated, and design parameters for different nodes.

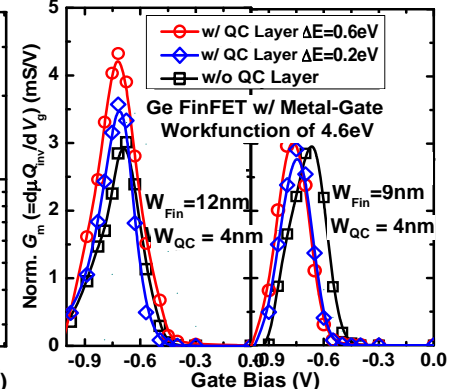| Node	22	14
W_{Fin} (nm)	12	9
EOT (nm)	1.0	0.85
t_{cap} (nm)	4	2.5
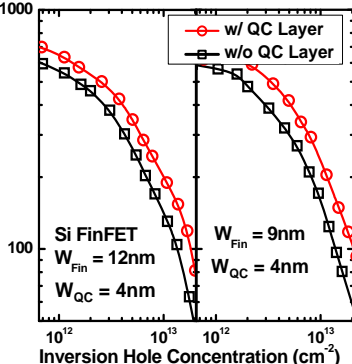
Fig. 10: Simulated Si FinFET hole mobilities for different nodes, w/ and w/o QC layers inserted.
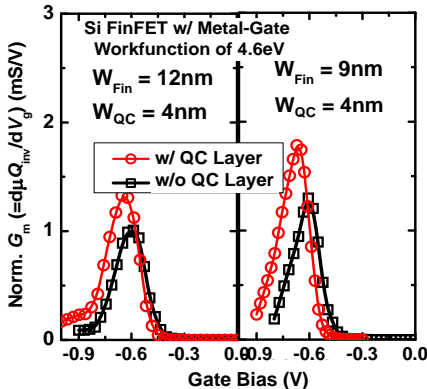
Fig. 11: Simulated Si P-channel FinFET normalized transconductance for different nodes, w/ and w/o QC layers inserted.

Fig. 12: Simulated Ge FinFET hole mobilities for different nodes, w/ and w/o QC layers inserted.

Fig. 13: Simulated Ge P-channel FinFET normalized transconductance for different nodes, w/ and w/o QC layers inserted.